On the Quantum Performance Evaluation of Two Distributed Quantum Architectures

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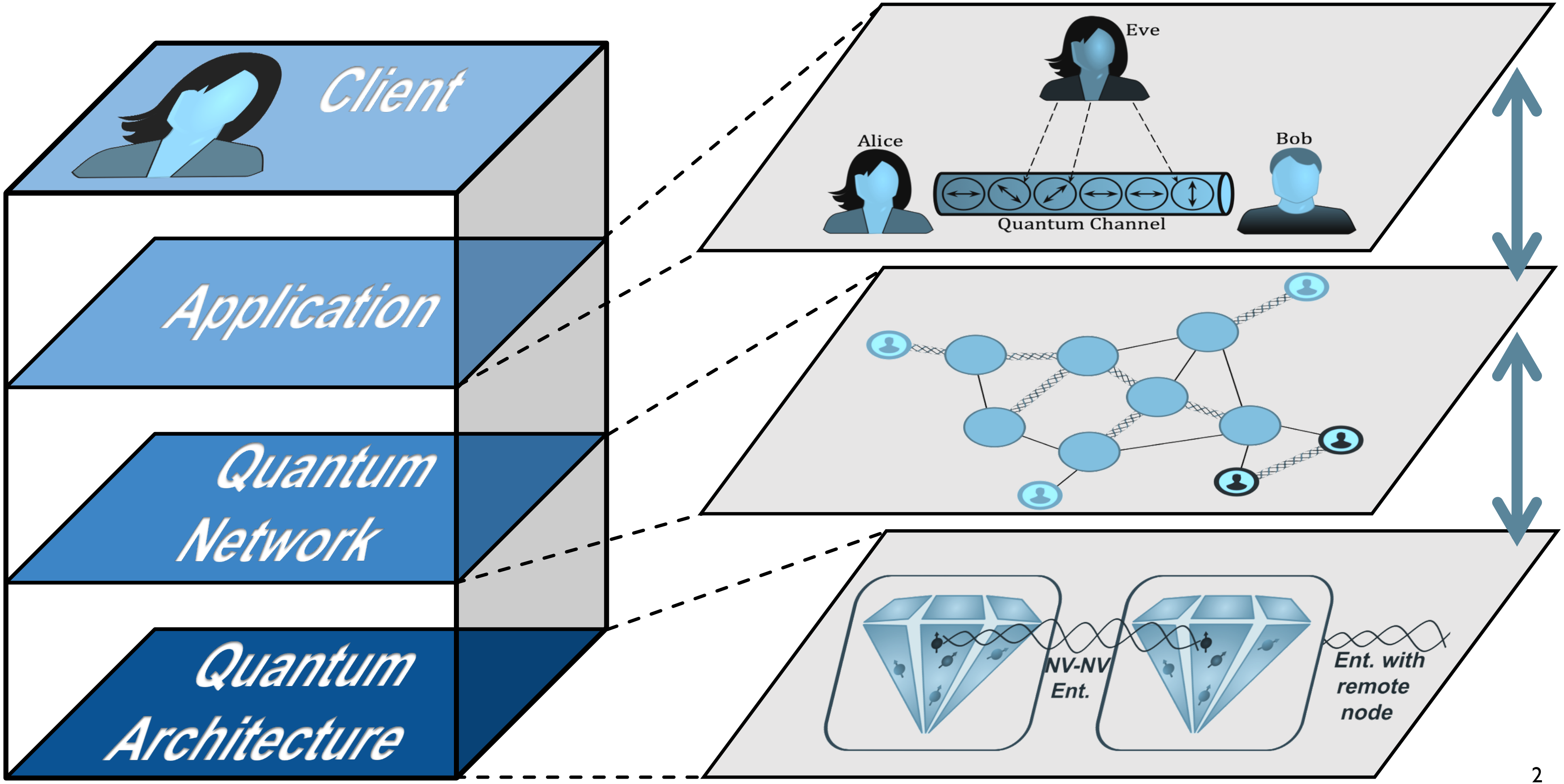
QuTech

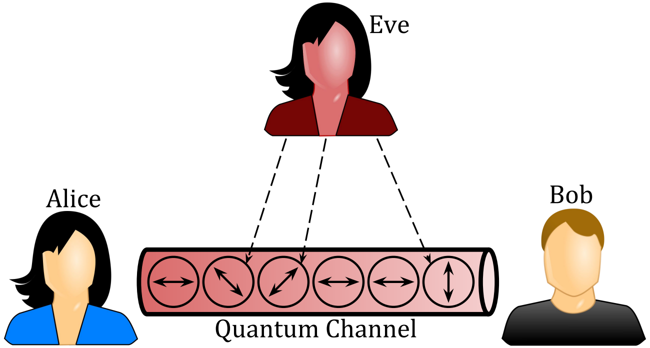
QuTech is a collaboration between TU Delft TNO

Distributed Quantum Application Stack



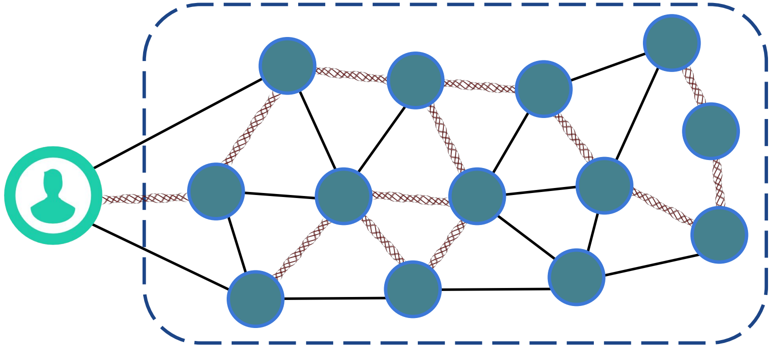
Diversity of Quantum Applications

Quantum Key Distribution



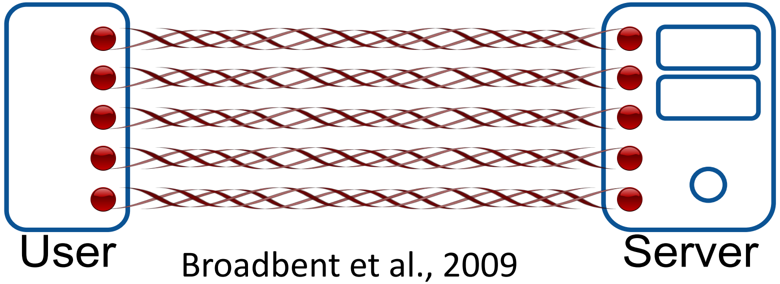
C. Bennett & G. Brassard, 1984; A. Ekert 1991

Quantum Computing Cluster



Jiang et al., 2018

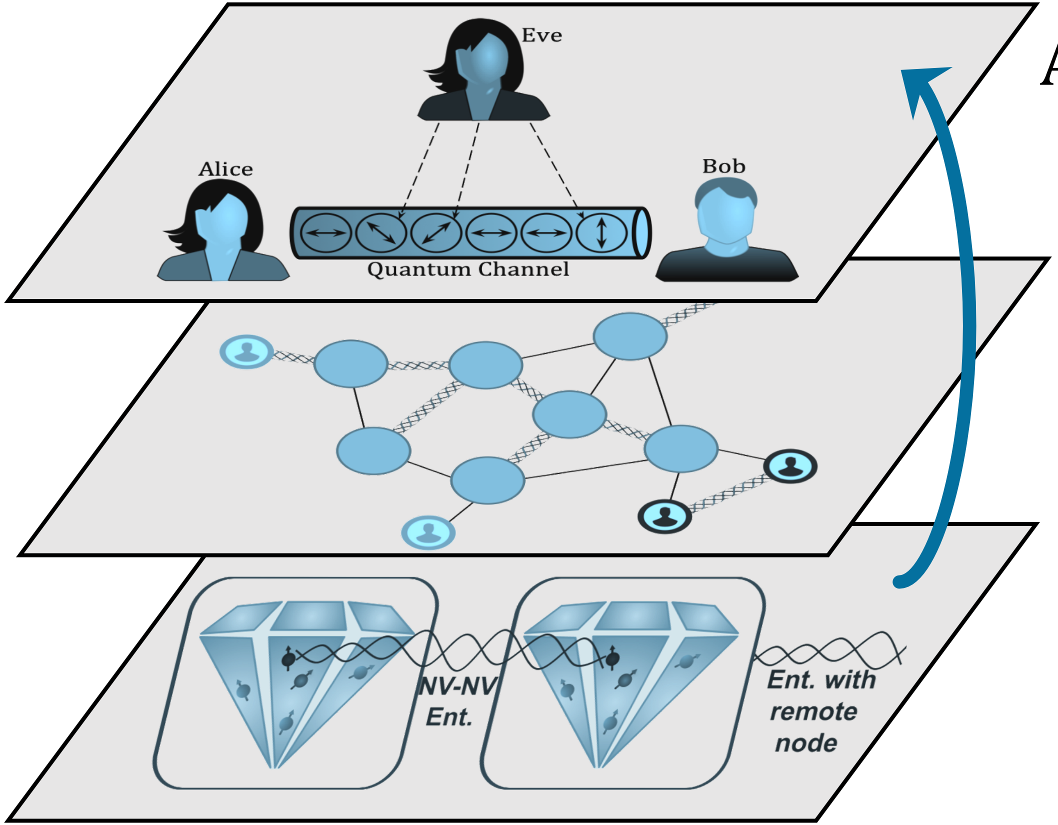
Secure Delegated Quantum Computing/ Blind Quantum Computing



Broadbent et al., 2009

Networking Heavy	Computation Heavy
QKD	Quantum Computing Cluster
Secure Delegated Quantum Computing/BQC	

How does distributed quantum architecture design affect application performance?

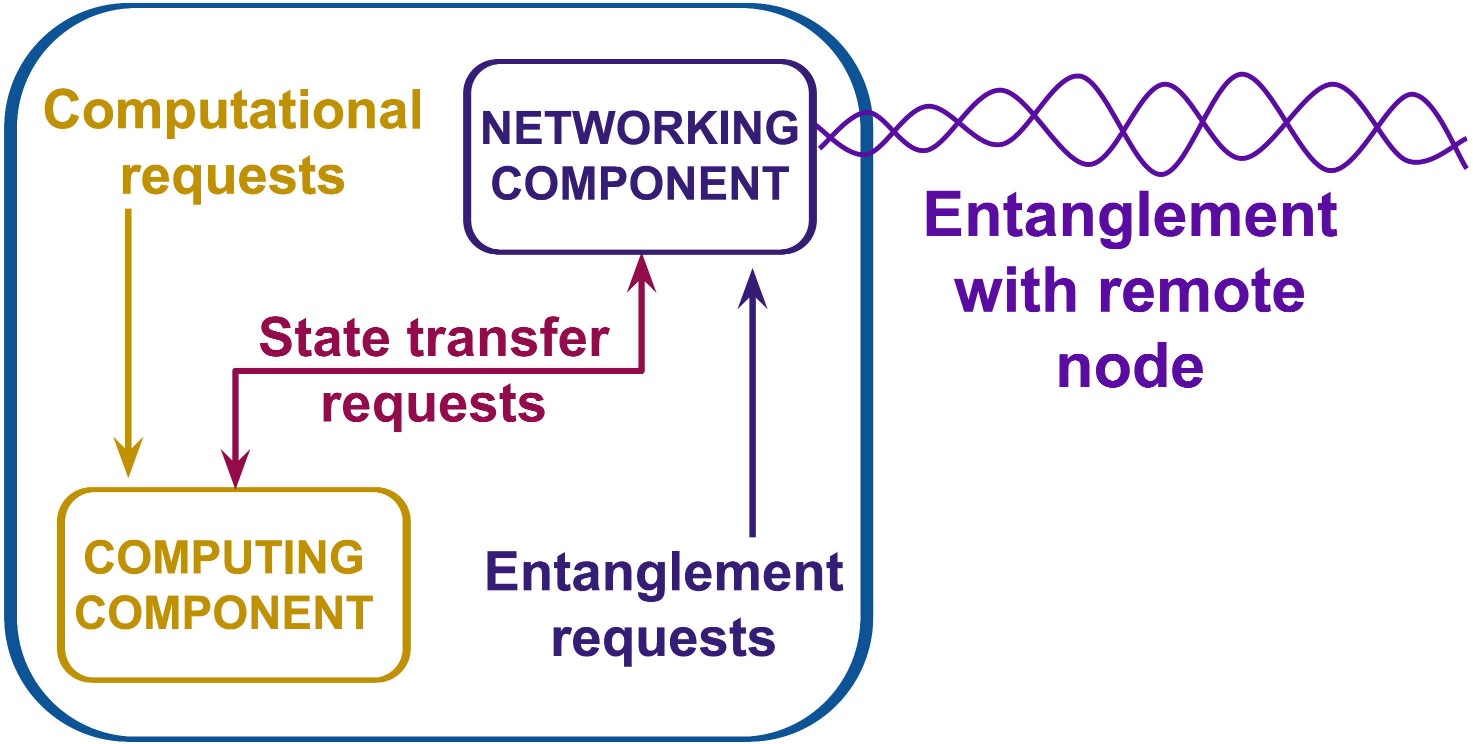


Application: computational & networking demands arrive at some ***request rate***

Network: provides entanglement at a certain ***generation rate***

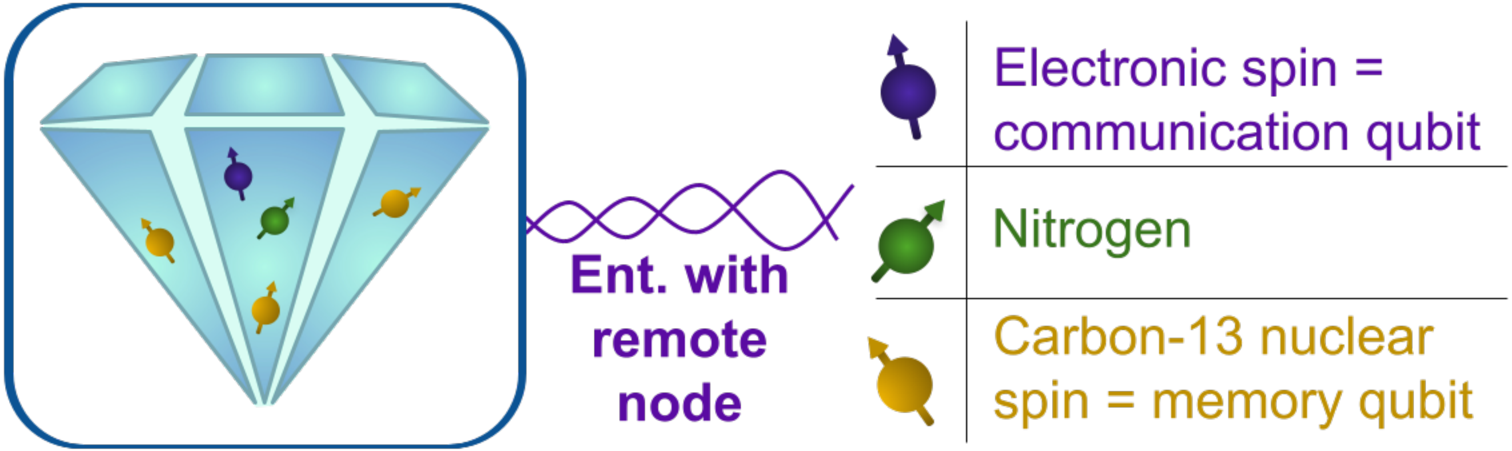
Architecture: performs processing at a certain ***computation rate***

A Possible Quantum Architecture



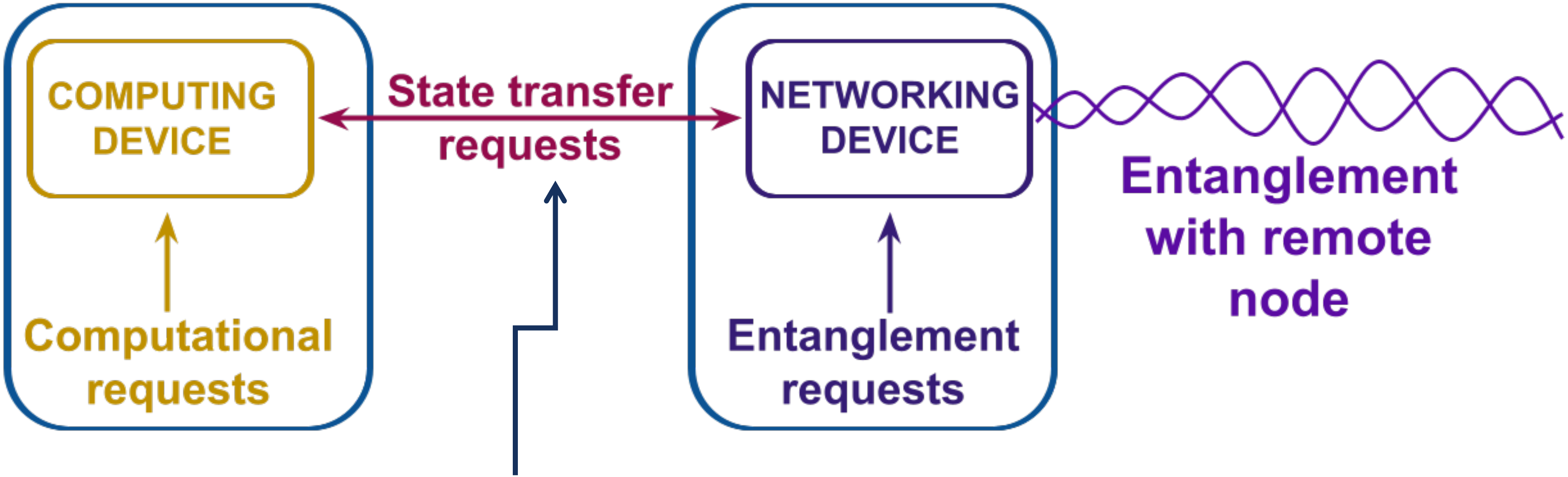
Quantum Processor Realization:

a single device used both for computing and networking (remote entanglement generation)



SD (single-device) design

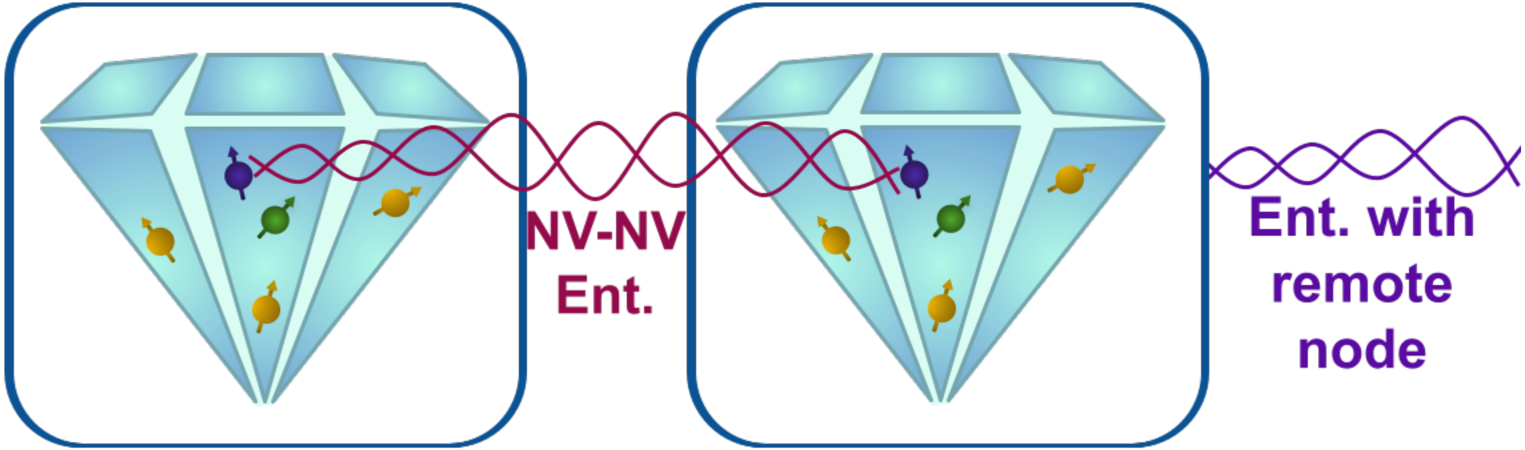
Another Architectural Model



inter-device interface for moving entangled qubits from net. to comp. device for processing

Quantum Processor Realization:

one device used solely for computation, the other solely for remote entanglement generation

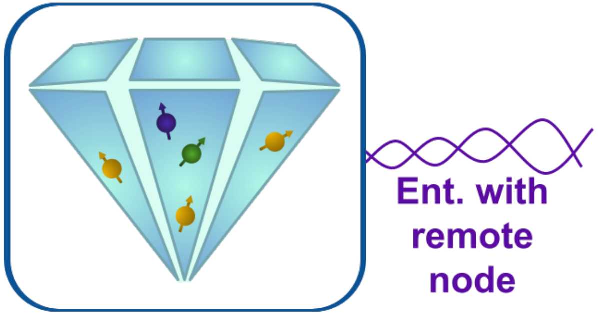


DD (double-device) design

Physical Restrictions

single-NV arch.

used for both computing and networking

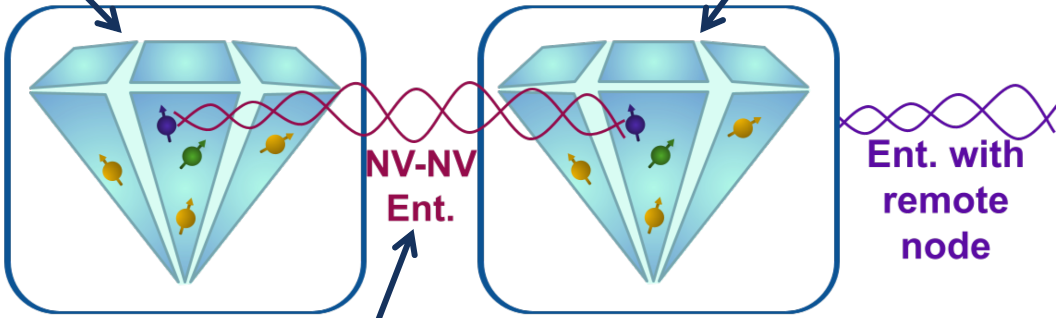


no computation allowed while entanglement generation attempt in progress

double-NV arch.

used for computing

used for networking

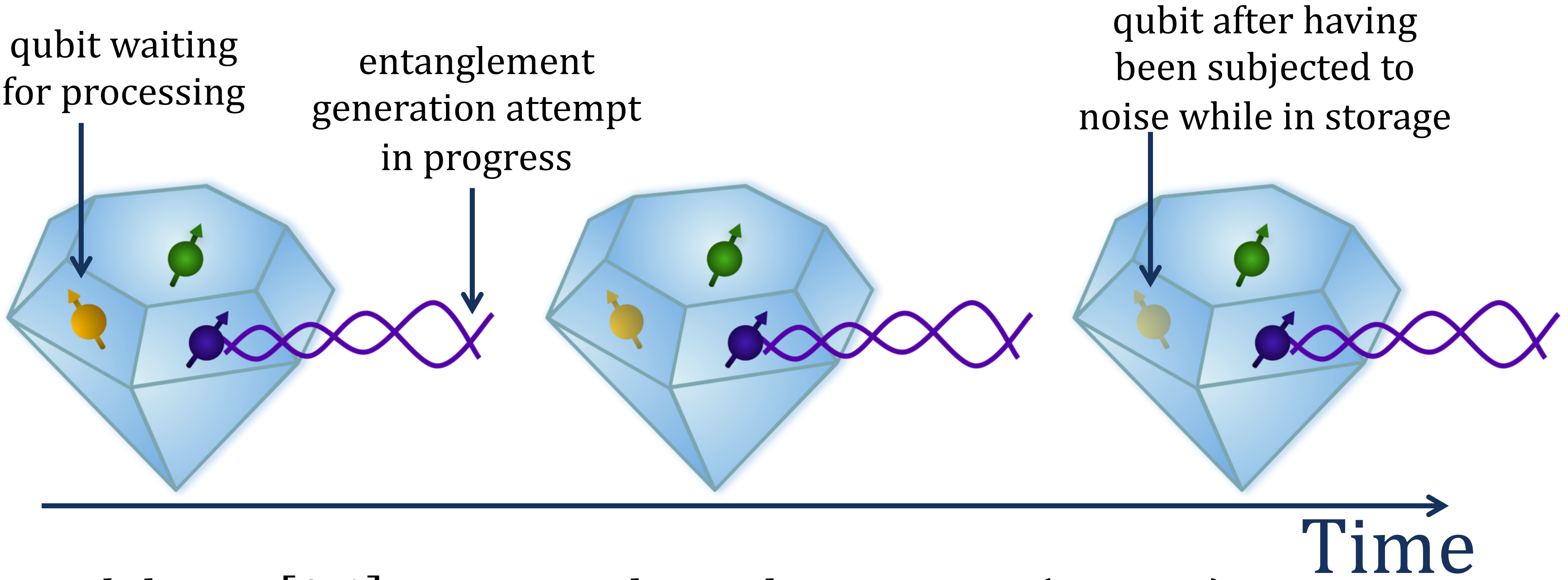


NV-NV entanglement needed to move entangled qubit state from one NV to another for processing

no computation or entanglement generation attempts allowed while move is in progress

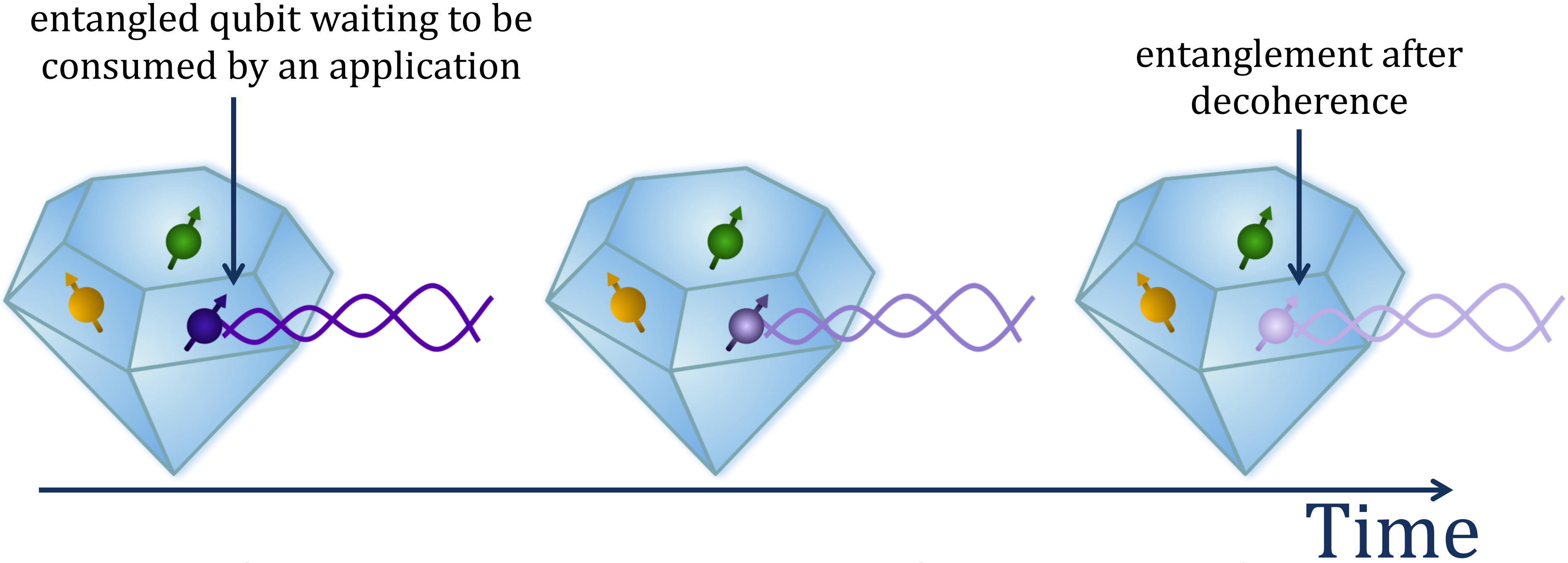
How do these restrictions affect quantum quality – *fidelity?*

Fidelity: a Quantum Performance Measure



Fidelity ∈ [0,1] measures how close a state (or gate) is to the target implementation.

Fidelity: a Quantum Performance Measure



Fidelity further decreases when transferring state of entangled qubit from communication to storage qubit.

Key Observations & Goals

- In systems with limited parallelism, qubits are **forced to wait**, resulting in **fidelity degradation**

Computing after storage ⟷ gate fidelity

Processing entanglement after storage ⟷ entanglement fidelity

- Goal: How are the ***gate fidelity*** and ***entanglement fidelity*** affected as a function of the waiting time?

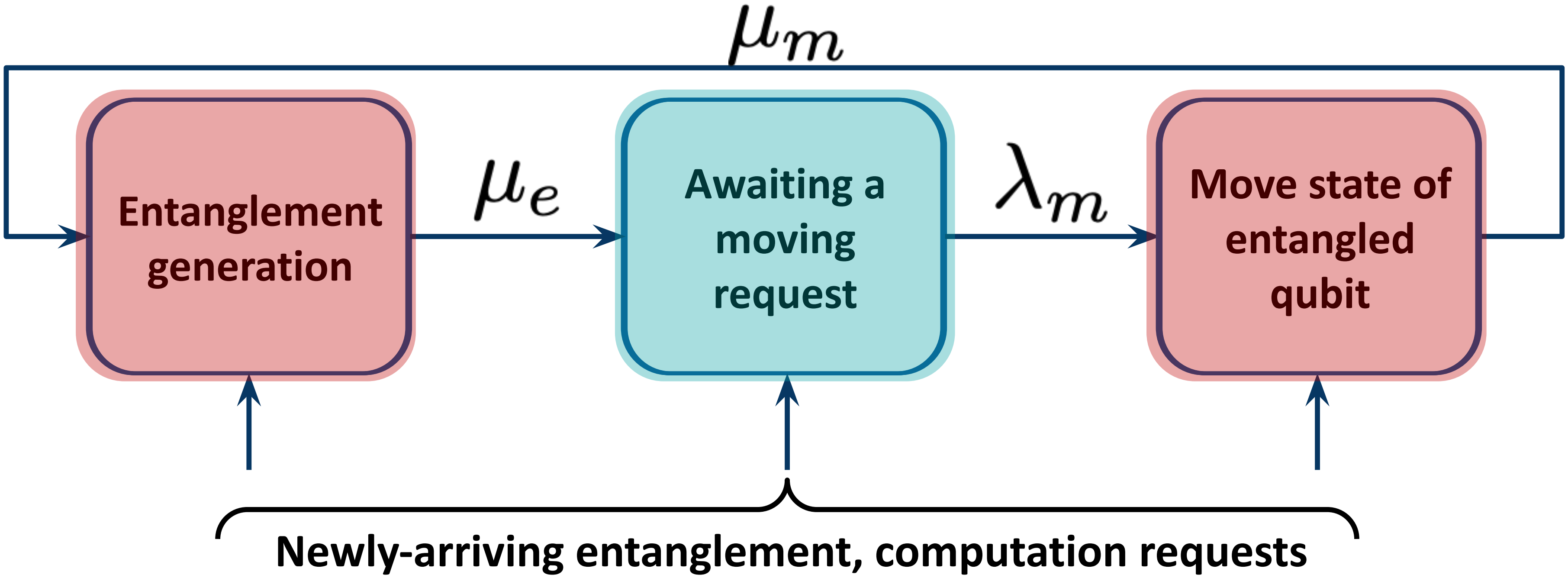
Our Contributions

- ❖ Mathematical formulas for *gate* and *entanglement* fidelities, for standard quantum noise models

- ❖ A Markov chain (QBD) modeling both designs, assuming:
    i. All requests arrive according to independent Poisson processes, completion times exp.-distr.
    ii. Local computation consumes negligible time

- ❖ Performance evaluation of the architectures, via analysis of the model as well as simulation

Simplified Representation of the Model



Analysis Example: Average Gate Fidelity

$\int$ (Choose an appropriate fidelity formula $\times$ Use Markov Chain to obtain waiting time distribution) $=$

$$1 - \frac{\lambda_e}{2\mu_m} + \frac{\lambda_e}{6}\left(\frac{2T_2}{\mu_m T_2 + 1} + \frac{T_1}{\mu_m T_1 + 1}\right)$$

entanglement request arrival rate

state transfer completion rate

characterize the memories

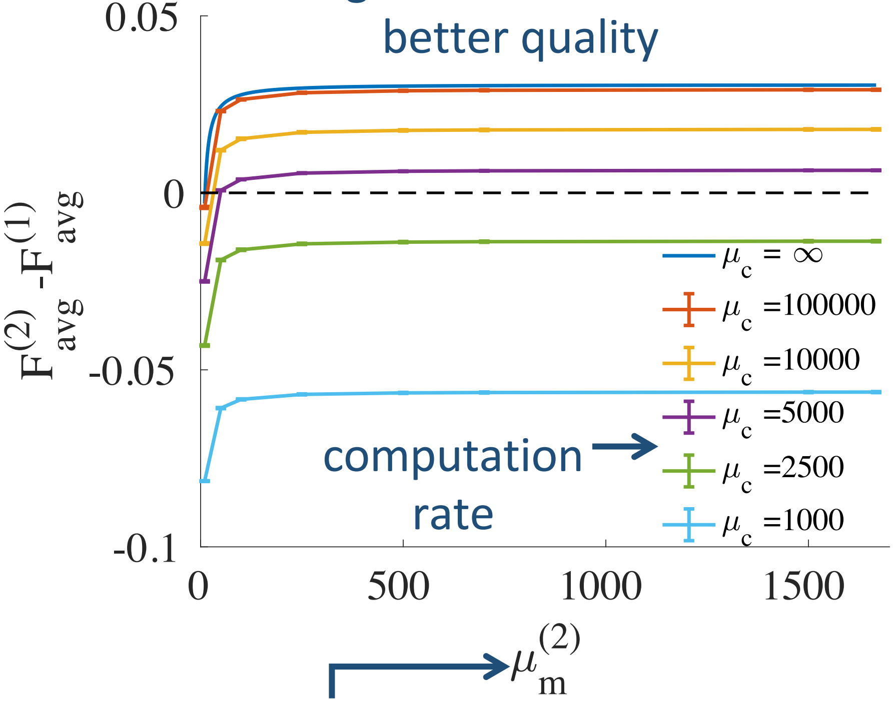
Results: Gate Fidelity

- More is more: two devices are better than one, if memories same

- Reason: qubits involved in computational jobs don't need to wait for entanglement generation when devices are separate

- Nevertheless: a single device with *better* memories may be the more economical option than two devices with poorer memories

Single-NV memories 5x better quality



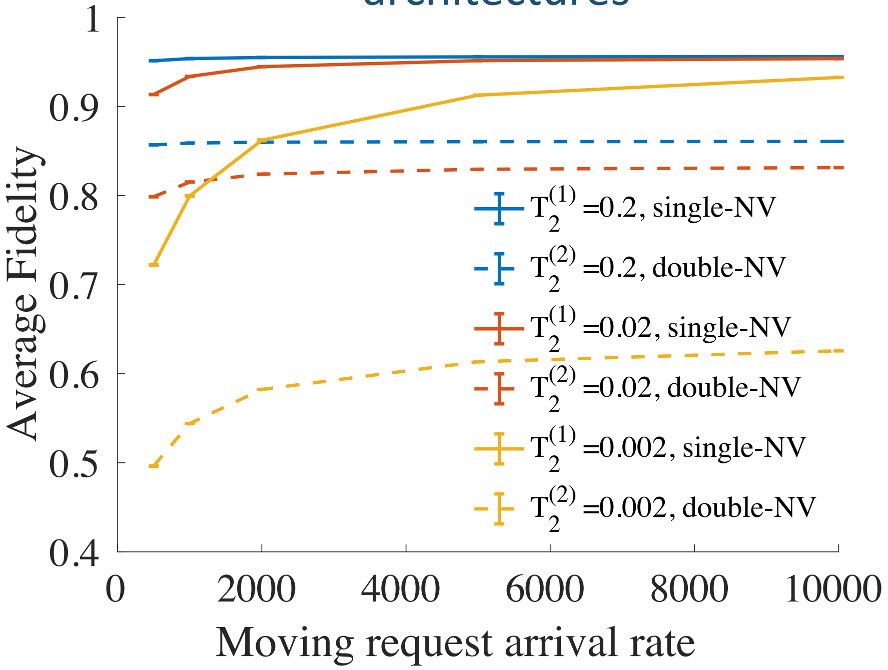
state transfer rate in double-NV arch.

Results: Post-Move Entanglement Fidelity

- Less is more: one device is more hospitable to entanglement fidelity, if gates imperfect

- Reason: state transfer across devices results in a more complex gate sequence, introducing more noise compared to state transfer in a single device (requiring only a local swap)

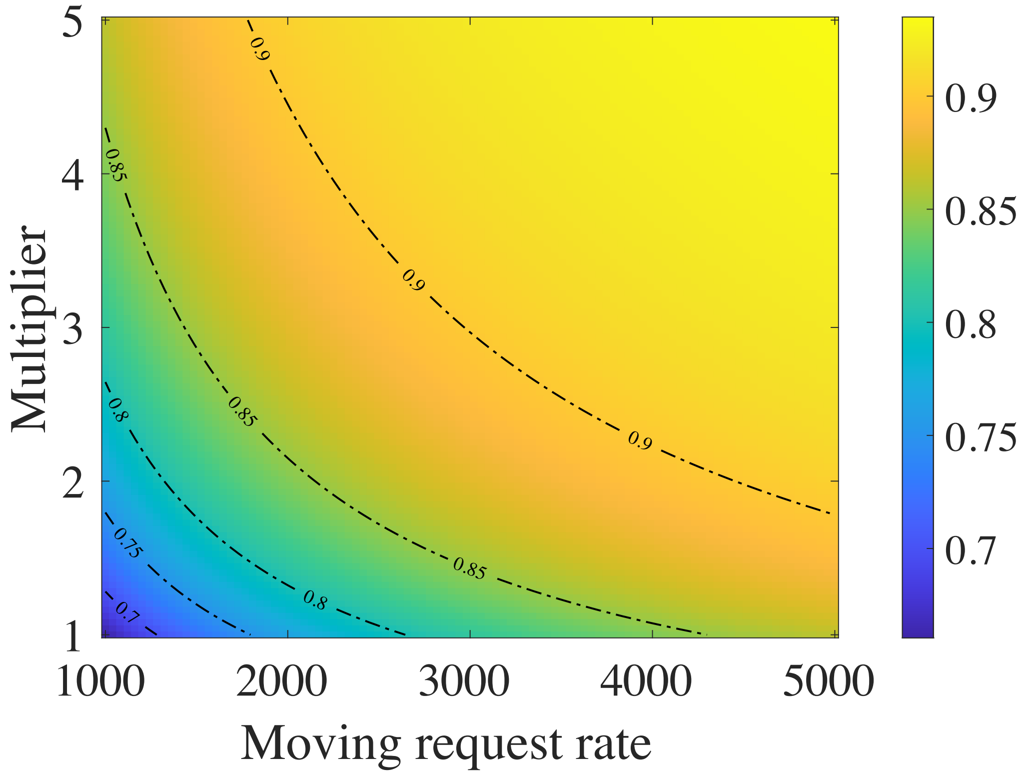
T_1 fixed at 2s for both architectures



How responsive should an application be with state transfers?

- Shown: single-device architecture *post-move fidelity* of entangled qubit
- Multiplier = 1 corresponds to T_1=0.00286s, T_2=0.001s

- The worse the memories, the more responsiveness is required from the application to move the state of the entangled qubit!



Main Findings

❖ For identical memory quality, two devices outperform one, in terms of ***gate fidelity***

❖ When the architectures rely on *imperfect gates*, the opposite is true for ***entanglement fidelity***

→ The **SD** architecture may be more suitable for ***network-heavy*** applications

→ The **DD** architecture may be more suitable for ***computation-heavy*** applications

❖ Sometimes, best to invest in quality, not quantity

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presented by **GAYANE VARDOYAN, NOVEMBER 10, 2021**

ON THE QUANTUM PERFORMANCE EVALUATION OF TWO DISTRIBUTED QUANTUM ARCHITECTURES

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